WHAT IS CLAIMED IS:

1. A method comprising:

a memory circuit receiving a data frame to be subsequently transmitted to a destination device via a first or second switching fabric, wherein the data frame comprises header and data fields, and wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

selecting a first multi-bit value [MASK] from a plurality of first multi-bit values according to the data contained in the one of the header fields, wherein the selected first multi-bit value comprises concatenated first and second multi-bit portions, wherein the bits of the first multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, and wherein the bits of the second multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics;

selecting a second multi-bit value [FPOE] from a plurality of second multi-bit values according to the data contained in the one of the header fields, wherein the bits of the first multi-bit value correspond, respectively, to the data ports of the first and second switching fabrics;

concatenating the second multi-bit value with itself to produce a concatenated second multi-bit value;

bit wise logically ANDing the selected first multi-bit value with the concatenated second multi-bit value to produce a third multi-bit value, wherein the third multi-bit comprises concatenated first and second portions;

selecting one of the first and second portions of the third multi-bit value;

adding the selected one of the first and second portions of the third multi-bit value to another header field of the received data frame;

transmitting the received data frame from the memory circuit to one of the first and second switching fabrics;

the data frame exiting the one of the first and second switching fabrics through one or more data ports thereof in accordance with the values of the bits of the selected one of the first and second portions of the third multi-bit value.

2. The method of claim 1 wherein the memory circuit is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

3. The method of claim 2 wherein the data frame is transmitted to the first switching fabric via the first data port or the second switching fabric via the second data port.

4. The method of claim 1 wherein the destination device is coupled to the first and second switching fabrics via third and fourth data ports, respectively, wherein the third data port is one of the first switching fabric data ports and the fourth data port is one of the second switching fabric data ports.

5. The method of claim 4 wherein the data frame is transmitted from the first switching fabric to the destination device via the third data port or the data frame is transmitted from the second switching fabric to the destination device via the fourth data port.

6. The method of claim 1 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of the data ports of the first and second switching fabrics through which the data frame may exit to reach the destination device.

7. The method of claim 4 wherein each bit of the first and second portions of the first multi-bit value is set to logical 1 or logical 0, wherein each of the first and second portions of the first multi-bit value comprises a first bit that corresponds to the fourth data port, and wherein only one of the two first bits is set to logical 1.

8. The method of claim 1 wherein only one bit of the selected one of the first and second portions of the third multi-bit value is set to logical 1, and wherein the one bit corresponds to a particular data port of the first and second switching fabric ports through which the data frame must exit to reach the destination device.

9. An apparatus comprising:

a memory circuit configured to receive a data frame to be subsequently transmitted to a destination device via a first or second switching fabric, wherein the data frame comprises header and data fields, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

a first circuit coupled to the memory circuit, wherein the first circuit is configured to receive data from one of the header fields, and wherein the first circuit is configured to produce a first multi-bit value in response to receiving the data;

a second circuit coupled to the memory circuit, wherein the second circuit is configured to receive the data, and wherein the second circuit is configured to produce a second multi-bit value in response to receiving the data;

a third circuit coupled to the first and second circuits, wherein the third circuit is configured produce a third multi-bit value in response to receiving the first and second multi-bit values from the first and second circuits, respectively, wherein the third circuit is configured to add the third multi-bit to another header field of the data frame;

wherein the memory circuit is configured to transmit the data frame to the first or second switching fabric after the third multi-bit value is added to the header field;

wherein the third multi-bit value identifies one of the data ports of the first or second switching fabrics through which the data frame must exit the switching fabric to reach the destination device.

10. The apparatus of claim 9 wherein the memory circuit is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

11. The apparatus of claim 9 further comprising the first and second switching fabrics and the destination device, wherein the destination device is coupled to the first and second switching fabrics via third and fourth data ports, respectively, wherein the third data port is one of the first switching fabric data ports and the fourth data port is one of the second switching fabric data ports.

12. The apparatus of claim 9 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of data ports of the first and second switching fabrics through which the data frame may exit to reach the destination device.

13. The apparatus of claim 9 wherein the first multi-bit value comprises concatenated first and second multi-bit portions, wherein the bits of the first multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, wherein the bits of the second multi-bit portion correspond, respectively, to the data ports of the first and second switching fabrics, wherein each of the first and second portions of the first multi-bit value comprises a first bit that corresponds to the fourth data port, and wherein only one of the two first bits is set to logical 1.

14. The apparatus of claim 9 wherein the third circuit comprises a concatenation circuit and an ANDing circuit, wherein the concatenation circuit is configured to concatenate the second multi-bit value with itself to produce a concatenated second multi-bit value, and wherein the ANDing circuit is configured to bit wise logically AND the first multi-bit value with the concatenated second multi-bit value.

15. The apparatus of claim 9 wherein only one bit of the third multi-bit value that is set to logical 1, and wherein the one bit corresponds to one data port of the first and second switching fabrics through which the data frame must exit to reach the destination device.

16. An apparatus comprising:

a buffer configured to receive a data frame to be transmitted to a destination device via a first or second switching fabric, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

a routing data generation circuit coupled to the buffer, wherein the routing data generation circuit is configured to generate and add routing data to the data frame received by the buffer, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;

wherein the buffer is configured to transmit the received data frame to the switching system after the routing data generation circuit adds the routing data to the data frame.

17. The apparatus of claim 16 the buffer is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

18. An apparatus comprising:

a memory circuit configured to receive a data frame to be transmitted to a destination device via a first or second switching fabric, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

means coupled to the memory circuit, to generate and add routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;

wherein the memory circuit is configured to transmit the received data frame to the switching system after the means adds the routing data to the data frame.

19. The apparatus of claim 18 wherein the memory circuit is coupled to the first and second switching fabrics via first and second data ports, respectively, wherein the first data port is one of the first switching fabric data ports and the second data port is one of the second switching fabric data ports.

20. A method comprising:

a memory circuit receiving a data frame to be transmitted to a destination device via first or second switching fabrics, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;

the memory circuit transmitting the received data frame to the switching system after the routing data has been added to the data frame.

21. A computer readable medium storing instructions executable by a computer system to implement a method, the method comprising:

a memory circuit of the computer system receiving a data frame to be transmitted to a destination device via first or second switching fabrics, wherein the first switching fabric comprises data ports through which data frames enter or exit the first switching fabric, and wherein the second switching fabric comprises data ports through which data frames enter or exit the second switching fabric;

generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the data ports of the first or second switching fabric through which the data frame will exit to reach the destination device;

the memory circuit transmitting the received data frame to the switching system after the routing data has been added to the data frame.